We claim:

1. In a cable modem termination system (CMTS) having at least a first active cable interface circuit transferring a first set of data signals to at least one cable modem using a first set of parameters stored within said first active cable interface circuit, said CMTS also having at least one spare interface circuit that is capable of communicating with a plurality of cable modems, a method of routing said first set of signals to said spare interface circuit comprised of the steps of:

a. copying at least a plurality of said first set of parameters for said first active cable interface circuit into said spare interface circuit;

b. on the failure of said first active cable interface circuit, routing said first set of data signals through said spare interface circuit according to said first set of parameters for said first active cable interface circuit that were copied into said spare interface circuit.

2. The method of claim 1 wherein said step of copying at least a plurality of said first set of parameters for said first active cable interface circuit into said spare interface circuit includes the step of: copying a plurality of parameter sets, for a plurality of active cable interface circuits into said spare interface circuit.

3. The method of claim 1 wherein said step of copying said first set of parameters for said first active cable interface circuit into said spare interface circuit includes the step of:

reading said first set of parameters from said first active cable interface circuit from memory comprising said first active cable interface circuit;

transferring the first set of parameters that were read from said first active cable interface into said spare interface circuit.

4. The method of claim 1 wherein said step of copying said first set of parameters for said first active cable interface circuit into said spare interface circuit includes the step of:

reading said first set of parameters from said first active cable interface circuit from a System Controller for said CMTS;

transferring the first set of parameters that were read from said System Controller for said CMTS into said spare interface circuit.

5. The method of claim 1 wherein said first set of parameters includes at least one of the following:

a. Downstream channel parameters;

b. Upstream channel parameters;

c. Service flow identification information;

d. Upstream channel identification information;

e. Upstream channel descriptor information.

f. At least one timing counter value.

6. In a cable modem termination system (CMTS) with a plurality of active cable interface circuits, each of which transfers data signals to a plurality of cable modems, each cable modem receiving said data signals through a corresponding one active cable interface circuit, the transfer of said data signals to each of said cable modems being enabled according to a set of service

parameters for each cable modem of said plurality of cable modems that is stored in the cable modem's corresponding active cable interface circuit, said CMTS also having at least one spare cable interface circuit that is capable of communicating with any of said plurality of cable modems, a method of routing said data signals to at least one of said cable modems through said spare cable interface circuit comprised of the steps of:

copying said service parameters of said first active cable interface circuit into said spare cable interface circuit;

on the failure of a first active cable interface circuit, routing data signals destined for said at least one cable modem through said spare cable interface circuit according to said first set of parameters for said first active cable interface copied into said spare cable interface circuit.

7. The method of claim 6 wherein said step of copying said service parameters of said first active cable interface circuit into said spare cable interface circuit includes the step of: copying a plurality of service parameter sets, for a plurality of active cable interface circuits into said spare cable interface circuit.

8. The method of claim 6 wherein said step of copying said service parameters for said first active cable interface circuit into said spare cable interface circuit includes the step of:

reading said service parameters for said active cable interface circuit from memory comprising said first active cable interface circuit;

transferring the service parameters that were read from said first active cable interface into said spare cable interface circuit.

9. The method of claim 6 wherein said step of copying said first set of parameters for said first active cable interface circuit into said spare cable interface circuit includes the step of:

reading said service parameters from said first active cable interface circuit from a System Controller for said CMTS;

transferring the service parameters that were read from said System Controller for said CMTS into said spare cable interface circuit.

10. The method of claim 6 wherein said service parameters includes at least one of the following:

g. Downstream channel parameters;

h. Upstream channel parameters;

i. Service flow identification information;

j. Upstream channel identification information;

k. Upstream channel descriptor information.

l. At least one timing counter value.

11. In a cable modem termination system (CMTS) with a plurality of cable interface circuits, each of which includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, a method of synchronizing the timing counter of a first cable interface circuit to the timing counter of a second cable interface circuit comprised of the steps of:

copying a first value of said timing counter of said first cable interface circuit into a storage device;

adding an offset to said first value to create a future timing counter value;

copying said future timing counter value into a storage device;

copying said future timing counter value from said storage device into said timing counter.

12. The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the step of:

a. waiting a predetermined length of time until said timing counter is substantially equal to said future timing counter value;

b. copying said future timing counter value from said storage device into said timing counter.

13. The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

c. waiting a predetermined length of time until said timing counter increases to a value substantially equal to said future timing counter value;

d. copying said future timing counter value from said storage device into said timing counter.

14. The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the step of:

e. triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said CMTS.

15. A cable modem termination system (CMTS) with a plurality of interface circuits, each of which includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, said CMTS comprising:

a System Controller means for: copying a first value of said timing counter of said first cable interface circuit into a storage device; adding an offset to said first value to create a future timing counter value; copying said future timing counter value from said storage device into said timing counter.

16. The CMTS of claim 15 wherein said System Controller means is a microprocessor.

17. The CMTS of claim 15 wherein said System Controller means is an application specific integrated circuit

18. The CMTS of claim 15 wherein said System Controller means is a field programmable gate array (FPGA).

19. The CMTS of claim 15 wherein said System Controller means is sequential logic.

20. In a synchronous clock system with a plurality of circuit cards, each of which includes a timing counter that provides timing signals, a method of synchronizing the timing counter of a first circuit card to the timing counter of a second circuit card comprised of the steps of:

copying a first value of said timing counter of said first circuit card into a storage device;

adding an offset to said first value to create a future timing counter value;

copying said future timing counter value from said storage device into said timing counter of said second card.

21. The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

a. waiting a predetermined length of time until said timing counter of said first circuit card is substantially equal to said future timing counter value;

b. copying said future timing counter value from said storage device into said timing counter of said second card.

22. The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter of said second card includes the steps of:

c. waiting a predetermined length of time until said timing counter increases to a value substantially equal to said future timing counter value;

d. copying said future timing counter value from said storage device into said timing counter of said second card.

23. The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter of said second card includes the step of:

e. triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said synchronous clock system.

24. A synchronous clock system having a plurality of circuit cards, each of which

includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, said synchronous clock system comprising:

a System controller means for: copying a first value of said timing counter of said first circuit card into a storage device; adding an offset to said first value to create a future timing counter value; and copying said future timing counter value into a storage device for a second circuit card.

25. The synchronous clock system of claim 24 wherein said System Controller means is a microprocessor.

26. The synchronous clock system of claim 24 wherein said System Controller means is an application specific integrated circuit

27. The synchronous clock system of claim 24 wherein said System Controller means is a field programmable gate array (FPGA).

28. The synchronous clock system of claim 24 wherein said System Controller means is sequential logic.